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|------|------------------------------------|---|------------------|
| TO   | Jose Alcala                        | DATE  | October 29, 2002 |
|      | NAME                               |   |                  |
|      | PTO                                | FAX #   | 703-746-4347     |
|      | COMPANY/FIRM                       |   |                  |
|      | NUMBER OF PAGES INCLUDING COVER: 3 | CONFIRM FAX: <input type="checkbox"/> YES <input type="checkbox"/> NO |                  |
| FROM | Remus F. Fetea                     | OUR REFERENCE   | 192711           |
|      | NAME                               |   |                  |
|      | 703-413-2383                       | YOUR REFERENCE  | 09/664,361       |
|      | DIRECT PHONE #                     |   |                  |

**MESSAGE**

Dear Examiner Alcala:

Please find enclosed, as per our telephone conversation of October 29, 2002, our proposed amendments to Claim 1 and the abstract.

With Best Regards,

Remus F. Fetea

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**DRAFT**

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**Marked-Up Copy**  
Serial No: 09/664,361  
Amendment Filed on:

IN THE CLAIMS

Please amend Claim 1 as shown in claim form below. A mark-up copy of the amended claim is attached.

--1. (Amended) A multilayered wiring substrate, comprising:

a plurality of multilayered wiring layers, at least one of said multilayered wiring layers [containing] comprising a signal wiring group made by a plurality of signal wirings disposed in parallel with one another; and

dummy wirings disposed on said at least one of said multilayered wiring outside said signal wiring group and in parallel to said signal wirings, at least one of said dummy wirings being disposed at each side of said signal wiring group that is parallel to said signal wirings. wherein

said dummy wirings have a same shape as said signal wirings.--

Claims 7-12. (New).

IN THE ABSTRACT

Page 23, lines 1-15, please amend the abstract to read as follows:

[ABSTRACT OF THE DISCLOSURE]

**DRAFT****ABSTRACT**

Each wiring layer of a multilayered wiring substrate [(100) comprises] includes signal wirings [(31a to 31n] disposed in parallel with one another, and dummy wirings [(31Da, 31Dn)] disposed at each side of the signal wiring group [(31)] made by signal wiring [(31b to 31m)], respectively. The dummy wirings [1Da, 31Dn)] have the same shape as the signal wirings [(31a to 31n)], and are disposed in parallel to the signal wirings [(31b to 31m)] at the same intervals as that in the signal wirings [(31a to 31n)]. Through holes [(40ab to 40mn)] are formed in the respective clearances among the signal wirings [(31a to 31n)]. Dummy through holes [(40Da, 40Dn)] having the same shape as the through holes [(40ab to 40mn)] are formed between the dummy at wiring [(31Da, 31Dn)] and signal wiring [(31a, 31n)]. A conductive layer is formed on the inner wall of the through hole [(40ab to 40mn, 40Da, 40D)]. [With the] The multilayered wiring substrate [(100), it] is able to reduce or eliminate the delay time difference between signals that propagate along the signal wirings.